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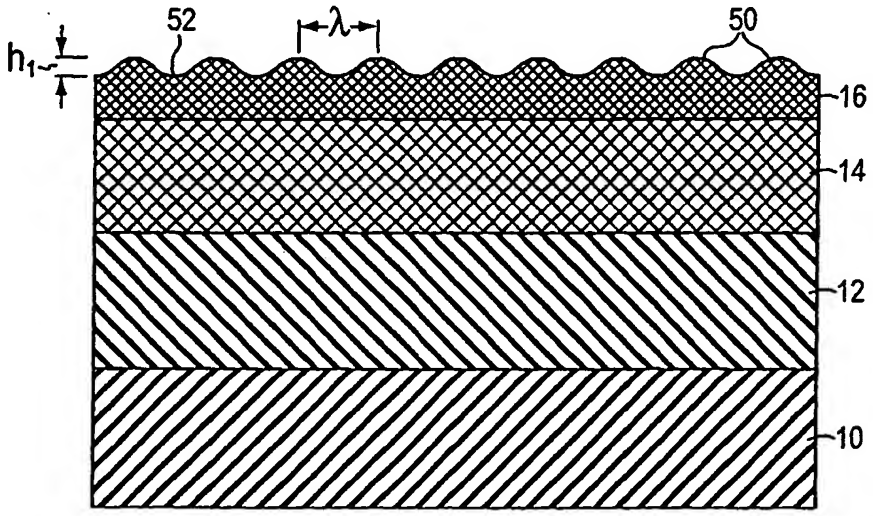

(57) Abstract: A structure and a method for forming the structure, the method including forming a compressively strained semiconductor layer, the compressively strained layer having a strain greater than or equal to 0.25%. A tensilely strained semiconductor layer is formed over the compressively strained layer. The compressively strained layer is substantially planar, having a surface roughness characterized in (I) having an average wavelength greater than an average wavelength of a carrier in the compressively strained layer or (ii) having an average height less than 10nm.

WO 03/015142 A2

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FORMATION OF PLANAR STRAINED LAYERS

Related Applications

This application claims the benefit of U.S. Provisional Application 60/310,346, filed August 6, 2001, the entire disclosure of which is hereby incorporated by reference herein.

Field of the Invention

This invention relates generally to semiconductor substrates and particularly to semiconductor substrates with strained layers.

Background

The recent development of silicon (Si) substrates with strained layers has increased the options available for design and fabrication of field-effect transistors (FETs). Enhanced performance of n-type metal-oxide-semiconductor (NMOS) transistors has been demonstrated with heterojunction metal-oxide-semiconductor field effect transistors (MOSFETs) built on substrates having strained silicon and relaxed silicon-germanium (SiGe) layers. Tensilely strained silicon significantly enhances electron mobilities. NMOS devices with strained silicon surface channels, therefore, exhibit improved performance with higher switching speeds. Hole mobilities are enhanced in tensilely strained silicon as well, but to a lesser extent for strain levels less than approximately 1.5%. Accordingly, equivalent enhancement of p-type metal-oxide-semiconductor (PMOS) device performance in such surface-channel devices presents a challenge.

Hole mobility enhancement has been demonstrated in highly strained SiGe layers. The formation of such highly strained layers is made difficult by the tendency of these layers to undulate, especially with increasing strain levels, i.e., with high Ge content. This undulation lowers hole mobilities, thereby offsetting the beneficial mobility enhancement provided by the strained layers.

The observed undulation arises from lattice mismatch with respect to an underlying layer, and increases in severity with formation temperature. Unfortunately, the formation of a tensilely strained layer made of, for example, Si, over the compressively strained layer is desirably carried out at a relatively high temperature, e.g., 550 °C, to achieve a commercially viable formation rate and uniformity.

Summary

The present invention facilitates formation of the tensilely strained layer at a relatively high average temperature, while keeping the compressively strained layer substantially planar. In accordance with the invention, the tensilely strained layer is initially grown at a relatively low temperature (i.e., sufficiently low to avoid undulations in the compressively strained layer) until a thin layer of the tensilely strained layer has been formed. It is found that this thin layer suppresses undulation in the compressively strained layer even at higher process temperatures that would ordinarily induce such undulation. As a result, formation of the tensilely strained layer may continue at these higher temperatures without sacrificing planarity.

In one aspect, therefore, the invention features a method for forming a structure based on forming a compressively strained semiconductor layer having a strain greater than or equal to 0.25%. A tensilely strained semiconductor layer is formed over the compressively strained layer. The compressively strained layer is substantially planar, having a surface roughness characterized by at least one of (i) an average roughness wavelength greater than an average wavelength of a carrier in the compressively strained layer and (ii) an average roughness height less than 10 nm.

One or more of the following features may also be included. The compressively strained layer may include at least one group IV element, such as at least one of silicon and germanium. The compressively strained layer may include >1% germanium. The tensilely strained layer may include silicon. The compressively strained layer may include at least one of a group III and a group V element. The compressively strained layer may include indium gallium arsenide, indium gallium phosphide, and/or gallium arsenide. The compressively strained layer may include at least one of a group II and a group VI element. The compressively strained layer may include zinc selenide, sulphur, cadmium telluride, and/or mercury telluride. The compressively strained layer may have a thickness of less than 500 Å, including less than 200 Å.

The compressively strained layer may be formed at a first temperature, and at least a portion of the tensilely strained layer may be formed at a second temperature, with the second temperature being greater than the first temperature. The tensilely strained layer may include silicon and the second temperature may be greater than 450 °C. A first portion of the tensilely strained layer may be formed at a first temperature and a second portion of the tensilely strained layer may be formed at the second temperature, the first temperature being sufficiently low to substantially avoid disruption of planarity, with the first portion of the tensilely strained layer maintaining the planarity of the compressively strained layer notwithstanding transition to the

second temperature.

The tensilely strained layer may be formed at a rate greater than 100 Å/hour. The compressively strained layer and/or the tensilely strained layer may formed by chemical vapor deposition. The wavelength of the surface roughness may be greater than 10 nanometers (nm).

In another aspect, the invention features a structure including a compressively strained semiconductor layer having a strain greater than or equal to 0.25% and a tensilely strained semiconductor layer disposed over the compressively strained layer. The compressively strained layer is substantially planar, having a surface roughness characterized by at least one of (i) an average roughness wavelength greater than an average wavelength of a carrier in the compressively strained layer and (ii) an average roughness height less than 10 nm.

One or more of the following features may also be included. The compressively strained layer may include a group IV element, such as at least one of silicon and germanium. The strain of the compressively strained layer may be greater than 1%. The compressively strained layer may have a thickness of less than 500 Å, including less than 200 Å. The wavelength of the surface roughness may be greater than 10 nm. The tensilely strained layer may include silicon.

The compressively strained layer may include at least one of a group III and a group V element. For example, the compressively strained layer may include indium gallium arsenide, indium gallium phosphide, and/or gallium arsenide.

The compressively strained layer may include at least one of a group II and a group VI element. For example, the compressively strained layer may include zinc selenide, sulphur, cadmium telluride, and/or mercury telluride.

The structure may also include a first transistor formed over the compressively strained layer. The first transistor may include a first gate dielectric portion disposed over a first portion of the compresssively strained layer, a first gate disposed over the first gate dielectric portion, the first gate comprising a first conducting layer, and a first source and a first drain disposed proximate the first gate and extending into the compressively strained layer. The first transistor may be an n-type metal-oxide-semiconductor field-effect transistor and the first source and first drain may include n-type dopants. The first transistor may be a p-type metal-oxide-semiconductor field-effect transistor and the first source and first drain may include p-type dopants.

The structure may also include a second transistor formed over the compressively strained layer. The second transistor may include a second gate dielectric portion disposed over a second portion of the compresssively strained layer, a second gate disposed over the second

gate dielectric portion, the second gate including a second conducting layer, and a second source and a second drain disposed proximate the second gate and extending into the compressively strained layer. The first transistor may be an n-type metal-oxide-semiconductor field-effect transistor, with the first source and first drain including n-type dopants, and the second transistor may be a p-type metal-oxide-semiconductor field-effect transistor, with the second source and second drain including p-type dopants.

Brief Description of Drawings

Figures 1 and 2 are schematic cross-sectional views of a semiconductor substrate with several semiconductor layers disposed thereon; and

Figure 3 is a schematic cross-sectional view of a semiconductor structure formed on a semiconductor substrate.

Detailed Description

Referring to Figure 1, which illustrates a structure amenable to use with the present invention, a substrate 10 is made of a semiconductor, such as silicon. Several layers collectively indicated at 11 are formed on substrate 10. Layers 11 may be grown, for example, in a chemical vapor deposition (CVD) system. In some embodiments, layers 11 are grown in an ultra-high vacuum chemical vapor deposition system (UHVCVD). In certain other embodiments, layers 11 may be grown in an atmospheric pressure CVD (APCVD) system or a low pressure CVD (LPCVD) system.

Layers 11 include a graded layer 12 disposed over substrate 10. Graded layer 12 may include Si and Ge with a grading rate of, for example, 10% Ge per micrometer (μm) of thickness, and a thickness T_1 of, for example, 2 - 9 μm. Graded layer 12 may be grown, for example, at 600 - 1100 °C. A relaxed layer 14 is disposed over graded SiGe layer 12. Relaxed layer 14 may include $Si_{1-x}Ge_x$ with a uniform composition, containing, for example, 20 - 90% Ge and having a thickness T_2 of, e.g., 0.2 - 2 μm. In an embodiment, T_2 is 1.5 μm. A virtual substrate 15 includes relaxed layer 14 and graded layer 12.

A compressively strained layer 16 including a semiconductor material is disposed over relaxed layer 14. In an embodiment, compressively strained layer 16 includes group IV elements, such as $Si_{1-y}Ge_y$, with a Ge content (y) higher than the Ge content (x) of relaxed $Si_{1-x}Ge_x$ layer 14. Compressively strained layer 16 contains, for example, 1 - 100% Ge and has a thickness T_3 of, e.g., 10 - 500 angstroms (Å). The Ge content (x) of relaxed $Si_{1-x}Ge_x$ layer 14 may be 20 – 90%, and the Ge content (y) of compressively strained $Si_{1-y}Ge_y$ layer 16 may be 28 – 100%. In some embodiments, compressively strained layer 16 has a thickness T_3 of less than

500 Å. In certain embodiments, T_3 is less than 200 Å.

In some embodiments, compressively strained layer 16 includes at least one group III and/or one group V element. Compressively strained layer 16 may include, for example, indium gallium arsenide, indium gallium phosphide, or gallium arsenide.

In alternative embodiments, compressively strained layer 16 includes at least one group II and/or one group VI element. Compressively strained layer may include, for example, zinc selenide, sulphur, cadmium telluride, or mercury telluride.

A tensilely strained layer 18 is disposed over compressively strained layer 16, sharing an interface 19 with compressively strained layer 16. In an embodiment, tensilely strained layer 18 is formed of silicon. Tensilely strained layer 18 has a thickness T_4 of, for example, 50 - 300 Å. In an embodiment, thickness T_4 is approximately 200 Å.

Substrate 10 with layers 11 typically has a threading dislocation density of $10^5/cm^2$.

The requirements for attaining a substantially planar compressively strained $Si_{1-y}Ge_y$ layer 16 and an acceptably high growth rate for tensilely strained Si layer 18 formed by CVD are sometimes mutually exclusive. For example, a high growth rate of tensilely strained Si layer 18 is more readily achieved by deposition at high CVD temperatures. Further, higher CVD temperatures reduce the incorporation of impurities and improve layer uniformity. More specifically, tensilely strained Si layer 18 may be deposited by the use of a silane (SiH_4) source gas. Adequate growth rates, i.e., > 0.01 Å/s with SiH_4, may be attained at 550 °C. On the other hand, germane (GeH_4) and SiH_4 may be used to deposit compressively strained $Si_{1-y}Ge_y$ layer 16. GeH_4 decomposes at approximately 400 °C. To remain planar after deposition, compressively strained $Si_{1-y}Ge_y$ layer 16 may need to be maintained at a relatively low temperature, i.e., less than the 550 °C temperature needed for subsequently achieving rapid Si deposition rates with SiH_4 to form tensilely strained Si layer 18.

As a result, maintaining adequate planarity of compressively strained $Si_{1-y}Ge_y$ layer 16 is a challenge, particularly with high Ge content, i.e., with y >40%. Si has a lattice constant of 5.431 Å and Ge has a lattice constant of 5.658 Å. The lattice mismatch between Si and Ge, therefore, is approximately 4%. Because of this lattice mismatch, a high Ge content leads to high compressive strain in compressively strained $Si_{1-y}Ge_y$ layer 16. High compressive strain may be desirable for attaining high carrier mobilities in subsequently fabricated devices.

Referring to Figure 2, the 4% difference in lattice constants of Si and Ge may lead to undulations 50 in a top surface 52 of compressively strained $Si_{1-y}Ge_y$ layer 16, particularly if the Ge content y is greater than 40%, and/or when the strain of compressively strained $Si_{1-y}Ge_y$ layer

16 is greater than .25% . Undulations 50 may form to partially accommodate the lattice mismatch between compressively strained $Si_{1-y}Ge_y$ layer 16 and relaxed layer 14. Undulations 50 may define a sinusoidal shape having a wavelength λ and a height h_1. Wavelength λ and height h_1 may depend on the Ge content of compressively strained $Si_{1-y}Ge_y$ layer 16, the lattice mismatch between compressively strained $Si_{1-y}Ge_y$ layer 16 and relaxed layer 14, and deposition conditions. Wavelength λ may be, for example, 1 – 100 nm, and height h_1 may be several nm, e.g., 5 nm. The sinusoidal shape of undulations 50 results in surface 52 having a surface roughness with wavelength λ. In an embodiment, the wavelength λ of the surface roughness is greater than a wavelength of a carrier in compressively strained $Si_{1-y}Ge_y$ layer 16. The surface roughness, therefore, does not reduce carrier mobility in compressively strained $Si_{1-y}Ge_y$ layer 16.

Referring to Figure 2 and also to Figure 1, a compressively strained $Si_{1-y}Ge_y$ layer 16 that is substantially planar may be grown as follows. Compressively strained $Si_{1-y}Ge_y$ layer 16 may be deposited at a first temperature low enough to enable formation of planar $Si_{1-y}Ge_y$ layers but not low enough to provide a suitably high deposition rate for tensilely strained Si layer 18. In the case of compressively strained $Si_{1-y}Ge_y$ layer 16 having a relatively high strain, e.g., greater than .25 % and/or with y> 40%, this deposition temperature for compressively strained $Si_{1-y}Ge_y$ layer 16 may be, e.g., 400 °C for UHVCVD using SiH_4 and GeH_4 source gases. The tensilely strained Si layer 18 may then be deposited in a two-step process. During the first step, the silicon source gas, e.g., SiH_4, is flowed while the growth temperature is slowly raised from a relatively low temperature, e.g., 400 °C, to a final desired temperature in which the silicon growth rate is acceptably high. The final desired temperature may be, e.g., > 450 °C, such as 550 °C, for UHVCVD using SiH_4 source gas. This step allows enough silicon to deposit at a low temperature to help stabilize the compressively strained $Si_{1-y}Ge_y$ layer 16 against strain-induced undulations, as explained below. Second, deposition of tensilely strained layer 18 may be completed at a faster rate at a second deposition temperature, e.g., a temperature greater than 450 °C, such as 550 °C, for UHVCVD using SiH_4 source gas. The deposition rate of tensilely strained layer 18 may be greater than 100 Å/hour. Another possible result of forming a substantially planar compressively strained $Si_{1-y}Ge_y$ layer 16 is an increase in wavelength λ of surface 52 of compressively strained $Si_{1-y}Ge_y$ layer 16. The increase in planarity may also be accompanied by a reduction in height h_1 of undulations to, e.g., less than 10 nm. After deposition of tensilely strained layer 18, compressively strained layer 16 has a surface roughness with wavelength λ greater than a wavelength of a carrier in compressively strained layer 16, e.g.,

greater than 10 nm.

A possible mechanism for formation of tensilely strained Si layer 18, deposited as described above, may be as follows. During the first step of the deposition of tensilely strained Si layer 18, surface 52 of compressively strained $Si_{1-y}Ge_y$ layer 16 is initially passivated by hydrogen atoms bonding to silicon and germanium during CVD when exposed to a hydrogen-containing source gas, such as SiH_4. The bond of hydrogen atoms to germanium, however, is relatively weak in comparison to the bond of hydrogen atoms to silicon. This bond strength difference is manifested, e.g., in the difference in the activation energy of decomposition of silane in UHVCVD (i.e., 2.22 eV) in comparison to the activation energy of decomposition of germane in UHVCVD (i.e., 1.68 eV). After passivation of surface 52, a surface exchange takes place in which a silicon atom from the SiH_4 source gas exchanges bonds to hydrogen with a germanium atom from compressively strained $Si_{1-y}Ge_y$ layer 16. The silicon atom thereby adheres to surface 52 of compressively strained $Si_{1-y}Ge_y$ layer 16, beginning formation of tensilely strained layer 18. Initially, a relatively fast growth rate of tensilely strained layer 18 may be attained at the relatively low temperature of approximately 400 °C because the exchange of Ge-H bonds with Si-H bonds is energetically favored and Ge atoms are directly at surface 52, or are relatively close to surface 52. Deposition at a higher temperature, however, may cause surface 52 to buckle excessively, resulting in undulations 50 with unacceptably short wavelength λ and/or high height h_1. As SiH_4 continues to flow and more Si atoms are deposited on surface 52 by exchange with Ge atoms, the deposition temperature may be raised. Buckling of surface 52 due to exposure to higher temperatures is prevented by the deposited Si atoms forming tensilely strained layer 18. Specifically, the deposited Si atoms physically suppress buckling of surface 52. As tensilely strained layer 18 becomes thicker, there is an increase in a migration path distance that Ge atoms in compressively strained $Si_{1-y}Ge_y$ layer 16 need to traverse to reach surface 52. This increase in Ge migration path distance becomes prohibitive, even at higher temperatures, resulting in Ge segregation from tensilely strained Si layer 18 and allowing the deposition of tensilely strained Si layer 18, substantially free of Ge. Consequently, initially depositing tensilely strained Si layer 18 at a relatively low temperature retards subsequent undulation formation, thereby facilitating completion of the deposition of tensilely strained Si layer at a higher temperature while maintaining the planarity of compressively strained layer 16.

In an alternative embodiment, during the first step of the deposition of tensilely strained Si layer 18, the flow of SiH_4 may be stopped during the increase in temperature, after the formation of a thin tensilely strained Si layer 18. The SiH_4 flow may then be resumed when the

deposition system reaches the desired higher temperature.

In some embodiments, a substantially planar compressively strained $Si_{1-y}Ge_y$ layer 16 may be formed, with compressively strained $Si_{1-y}Ge_y$ layer 16 having a strain greater than 1%, by using the two-step silicon deposition process described above.

In another embodiment, compressively strained layer 16 may be formed as follows. Compressively strained $Si_{1-y}Ge_y$ layer 16 having a relatively low Ge content is deposited on relaxed $Si_{1-x}Ge_x$ layer 14, e.g., $y \sim 0.4 - 0.6$, under relatively light compressive strain, e.g., $y - x \approx 0.2$. In this embodiment, device layers 20, including compressively strained $Si_{1-y}Ge_y$ layer 16 and tensilely strained Si layer 18, may be deposited at a temperature that permits deposition of planar compressively strained $Si_{1-y}Ge_y$ layer 16 and simultaneously provides an acceptably high growth rate, e.g., > 0.01 Å/s, for tensilely strained Si layer 18. This temperature may be, e.g., 550 °C in ultrahigh vacuum chemical vapor deposition using SiH_4 and GeH_4 source gases.

Referring to Figure 3 as well as to Figures 1 and 2, a first transistor 60 and a second transistor 62 may be formed over a substantially planar compressively strained semiconductor layer 16 having a strain greater than or equal to 0.25%. Tensilely strained semiconductor layer 18 is disposed over compressively strained layer 16. First transistor 60 includes a first gate dielectric portion 64 disposed over a first portion 66 of compressively strained semiconductor layer 16. First dielectric portion 64 may be formed of a dielectric such as, e.g., silicon dioxide. A first gate 68 is disposed over first gate dielectric portion 64. First gate 68 includes a first conducting layer, such as, e.g., doped polysilicon. First transistor 60 also includes a first source 70 and a first drain 72 (defined for purposes of illustration by the interior boundaries), disposed proximate first gate 68 and extending into compressively strained layer 16. In an embodiment, first transistor 60 is a PMOS field-effect transistor, and first source 70 and first drain 72 are formed by the introduction of p-type dopants, such as boron. In an alternative embodiment, first transistor 60 is an NMOS field-effect transistor, and first source 70 and first drain 72 are formed by the introduction of n-type dopants, such as phosphorus or arsenic.

Second transistor 62 includes a second gate dielectric portion 74 disposed over second portion 76 of compressively strained semiconductor layer 16. Second dielectric portion 74 may be formed of a dielectric such as, e.g., silicon dioxide. A second gate 78 is disposed over second gate dielectric portion 74. Second gate 78 includes a second conducting layer, such as, e.g., doped polysilicon. Second transistor 62 also includes a second source 80 and a second drain 82 (defined for purposes of illustration by the interior boundaries), disposed proximate second gate 78 and extending into compressively strained layer 16. Second transistor 62 may be an NMOS

field-effect transistor. Second source 80 and second drain 82 may be formed by the introduction of n-type dopants, such as phosphorus or arsenic.

In an embodiment, first transistor 60 is a PMOS field-effect transistor with first source 70 and first drain 72 including p-type dopants, and second transistor 62 is an NMOS field-effect transistor with second source 80 and second drain 82 including n-type dopants. Together, first transistor 60 and second transistor 62 form a complementary metal-oxide-semiconductor (CMOS) device.

The functionality of first and second transistors 60, 62 is enhanced by the use of substrate 10 with a substantially planar compressively strained semiconductor layer 16. The planarity of compressively strained semiconductor layer 16 enhances mobility of carriers within compressively strained layer 16, thereby enabling faster speeds during operation of first and second transistors 60, 62.

The invention may be embodied in other specific forms without departing from the spirit of essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced herein.

Claims

1. A method for forming a structure, the method including:

forming a compressively strained semiconductor layer, the compressively strained layer having a strain greater than or equal to 0.25%; and

forming a tensilely strained semiconductor layer over the compressively strained layer,

wherein the compressively strained layer is substantially planar, having a surface roughness characterized by at least one of (i) an average roughness wavelength greater than an average wavelength of a carrier in the compressively strained layer and (ii) an average roughness height less than 10 nm.

2. The method of claim 1, wherein the compressively strained layer comprises at least one group IV element.

3. The method of claim 1, wherein the compressively strained layer comprises at least one of silicon and germanium.

4. The method of claim 3, wherein the compressively strained layer comprises >1% germanium.

5. The method of claim 1, wherein the tensilely strained layer comprises silicon.

6. The method of claim 1, wherein the compressively strained layer comprises at least one of a group III and a group V element.

7. The method of claim 6, wherein the compressively strained layer comprises indium gallium arsenide.

8. The method of claim 6, wherein the compressively strained layer comprises indium gallium phosphide.

9. The method of claim 6, wherein the compressively strained layer comprises gallium arsenide.

10. The method of claim 1, wherein the compressively strained layer comprises at least one of a group II and a group VI element.

11. The method of claim 10, wherein the compressively strained layer comprises zinc

selenide.

12. The method of claim 10, wherein the compressively strained layer comprises sulphur.

13. The method of claim 10, wherein the compressively strained layer comprises cadmium telluride.

14. The method of claim 10, wherein the compressively strained layer comprises mercury telluride.

15. The method of claim 1, wherein the compressively strained layer has a thickness of less than 500 Å.

16. The method of claim 15, wherein the compressively strained layer has a thickness of less than 200 Å.

17. The method of claim 1, wherein the compressively strained layer is formed at a first temperature, at least a portion of the tensilely strained layer is formed at a second temperature, and the second temperature is greater than the first temperature.

18. The method of claim 17, wherein the tensilely strained layer comprises silicon and the second temperature is greater than 450 °C.

19. The method of claim 17, wherein forming the tensilely strained layer at a second temperature includes initially forming a first portion of the tensilely strained layer at the first temperature and forming a second portion of the tensilely strained layer at the second temperature, the first temperature being sufficiently low to substantially avoid disruption of planarity, the first portion of the tensilely strained layer maintaining the planarity of the compressively strained layer notwithstanding transition to the second temperature.

20. The method of claim 1, wherein the tensilely strained layer is formed at a rate greater than 100 Å/hour.

21. The method of claim 1, wherein the compressively strained layer is formed by chemical vapor deposition.

22. The method of claim 1, wherein the tensilely strained layer is formed by chemical vapor deposition.

23. The method of claim 1, wherein the wavelength of the surface roughness is greater than 10 nanometers.

24. A structure comprising:

a compressively strained semiconductor layer having a strain greater than or equal to 0.25%; and

a tensilely strained semiconductor layer disposed over the compressively strained layer,

wherein the compressively strained layer is substantially planar, having a surface roughness characterized by at least one of (i) an average roughness wavelength greater than an average wavelength of a carrier in the compressively strained layer and (ii) an average roughness height less than 10 nm.

25. The structure of claim 24, wherein the compressively strained layer comprises a group IV element.

26. The structure of claim 25, wherein the compressively strained layer comprises at least one of silicon and germanium.

27. The structure of claim 26, wherein the strain of the compressively strained layer is greater than 1%.

28. The structure of claim 24, wherein the compressively strained layer has a thickness of less than 500 Å.

29. The structure of claim 28, wherein the compressively strained layer has a thickness of less than 200 Å.

30. The structure of claim 24, wherein the wavelength of the surface roughness is greater than 10 nanometers.

31. The structure of claim 24, wherein the tensilely strained layer comprises silicon.

32. The structure of claim 24, wherein the compressively strained layer comprises at least one of a group III and a group V element.

33. The structure of claim 32, wherein the compressively strained layer comprises indium gallium arsenide.

34. The structure of claim 32, wherein the compressively strained layer comprises indium gallium phosphide.

35. The structure of claim 32, wherein the compressively strained layer comprises gallium arsenide.

36. The structure of claim 24, wherein the compressively strained layer comprises at least one of a group II and a group VI element.

37. The structure of claim 36, wherein the compressively strained layer comprises zinc selenide.

38. The structure of claim 36, wherein the compressively strained layer comprises sulphur.

39. The structure of claim 36, wherein the compressively strained layer comprises cadmium telluride.

40. The structure of claim 36, wherein the compressively strained layer comprises mercury telluride.

41. The structure of claim 24, further comprising:

a first transistor formed over the compressively strained layer, the first transistor including:

(i) a first gate dielectric portion disposed over a first portion of the compresssively strained layer,

(ii) a first gate disposed over the first gate dielectric portion, the first gate comprising a first conducting layer, and

(iii) a first source and a first drain disposed proximate the first gate and extending into the compressively strained layer.

42. The structure of claim 41, wherein the first transistor is an n-type metal-oxide-semiconductor field-effect transistor and the first source and first drain comprise n-type dopants.

43. The structure of claim 41, wherein the first transistor is a p-type metal-oxide-semiconductor field-effect transistor and the first source and first drain comprise p-type dopants.

44. The structure of claim 41, further comprising:

a second transistor formed over the compressively strained layer, the second transistor including:

(i) a second gate dielectric portion disposed over a second portion of the compresssively strained layer,

(ii) a second gate disposed over the second gate dielectric portion, the second gate comprising a second conducting layer, and

(iii) a second source and a second drain disposed proximate the second gate and extending into the compressively strained layer,

wherein the first transistor is an n-type metal-oxide-semiconductor field-effect transistor, the first source and first drain comprise n-type dopants, the second transistor is a p-type metal-oxide-semiconductor field-effect transistor, and the second source and second drain comprise p-type dopants.

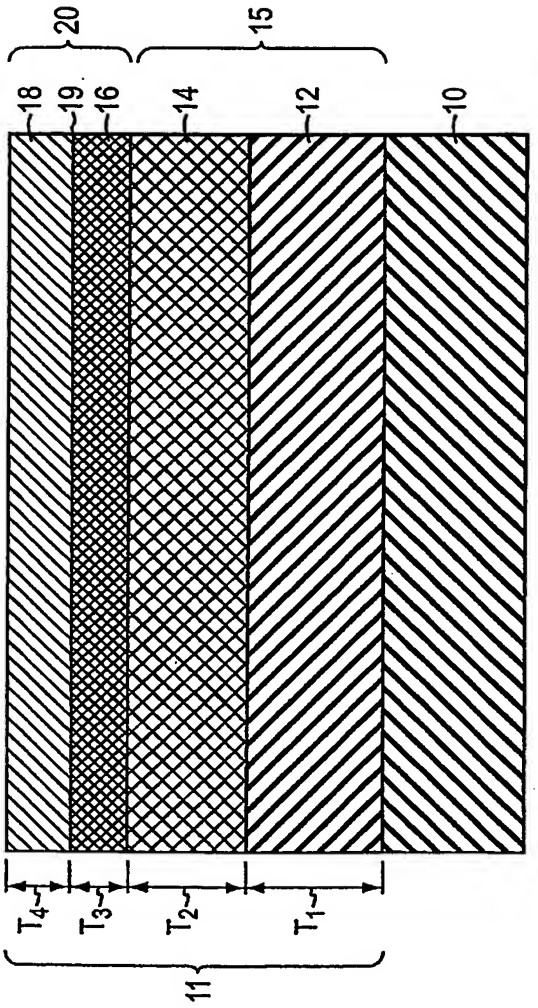

FIG. 1

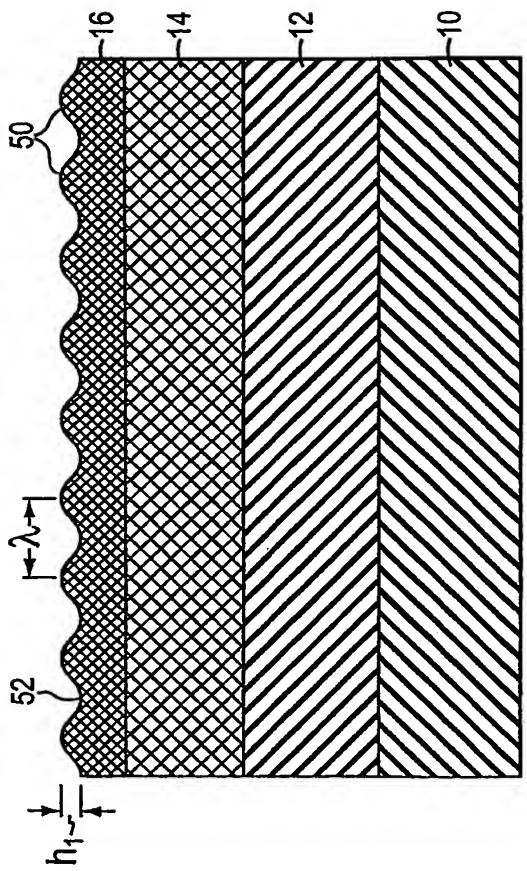

FIG. 2

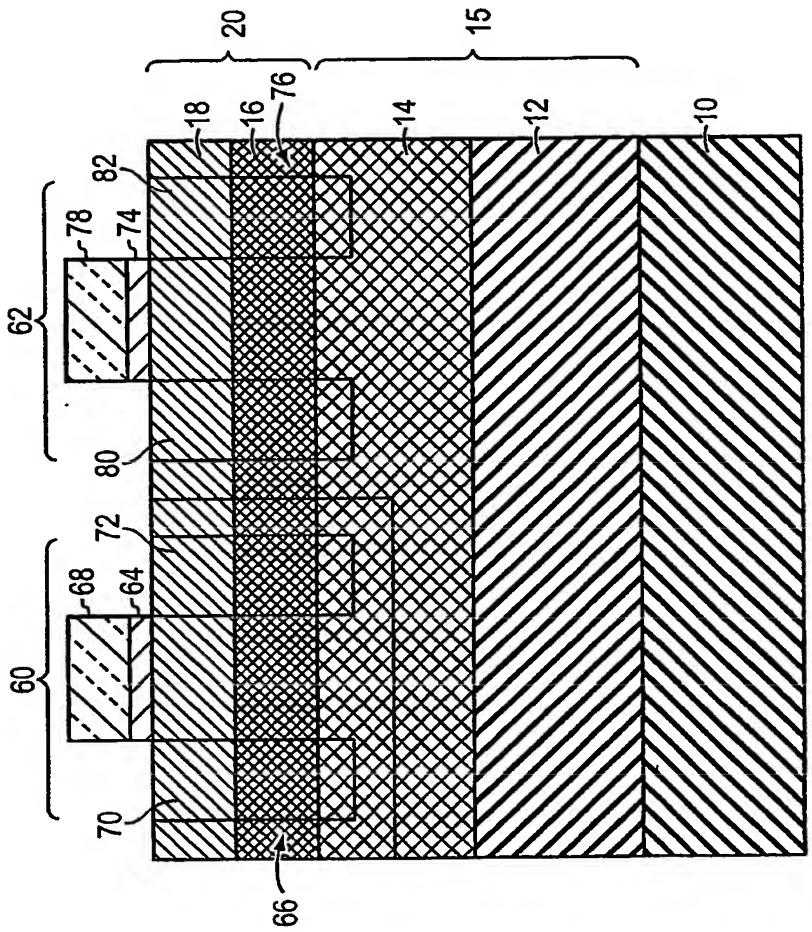

FIG. 3